Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT –**
2. **INPUT +**
3. **OSC OUT**
4. **(+) CL SENSE**
5. **(-) CL SENSE**
6. **RT**
7. **CT**
8. **GND**
9. **COMP**
10. **S/D**
11. **EA**
12. **CA**
13. **CB**
14. **EB**
15. **VIN**
16. **VREF**

**.082”**

**.076”**

**2 1 16 15**

**3**

**4**

**5**

**6**

**7 8 9 10**

**14**

**13**

**12**

**11**

**1524**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si or SiN2**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 1524**

**APPROVED BY: DK DIE SIZE .076” X .082” DATE: 10/6/22**

**MFG: UNITRODE/TI THICKNESS .011” P/N: UC1524**

**DG 10.1.2**

#### Rev B, 7/1